IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application.

Claim 1 (Currently Amended) A comparator comprising:

a circuit for setting a trip point of a rising edge of an input signal according to a value of [an] a positive external voltage reference; and

at least two transistors, in said circuit, for setting a trip point of a falling edge of said input signal according to a width-to-length ratio of said at least two transistors[.],

wherein said comparator cycles between an analog circuit and a digital circuit, and

wherein in said analog circuit, one of said at least two transistors is a tail current source transistor, and wherein said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.

Claims 2-3 (Canceled).

Claim 4 (Original) The comparator of claim 3, further comprising a plurality of transmission gates in said circuit, wherein said rise in said input signal causes said comparator to appear as a differential pair in an open loop configuration.

Claim 5 (Currently Amended) The comparator of claim 2, wherein in said digital circuit, said input signal is at an input voltage greater than said positive external [reference] voltage reference.

Claim 6 (Original) The comparator of claim 5, further comprising a plurality of transmission gates in said circuit, wherein said input signal causes said comparator to appear as an asymmetric inverting Schmitt trigger.

Claim 7 (Original) The comparator of claim 1, wherein said at least two transistors comprises:

a first transistor of length (L_x) and a width of (W_x); and

a second transistor of length (L_y) and a width of (W_y),

wherein said width-to-length ratio equals $(W_x L_y)/(W_y L_x)$, and

wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio.

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Claim 8 (Original) The comparator of claim 7, wherein said trip point of a falling edge of an input signal decreases by decreasing said width-to-length ratio.

Claim 9 (Original) The comparator of claim 7, wherein said trip point of a falling edge of an input signal increases by increasing said width-to-length ratio.

Claim 10 (Currently Amended) A comparator comprising:

a circuit for setting a trip point of a rising edge of an input signal according to a value of an external voltage reference; and

at least two transistors, in said circuit, for setting a trip point of a falling edge of the input signal according to a width-to-length ratio of said at least two transistors,

wherein said comparator cycles between an analog circuit and a digital circuit,

wherein said trip point of a falling edge of an input signal decreases by decreasing said width-to-length ratio, [and]

wherein said trip point of a falling edge of an input signal increases by increasing said width-to-length ratio[.], and

wherein said analog circuit further comprises a tail current source transistor, and wherein said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.

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Claim 11 (Original) The comparator in claim 10, wherein said at least two transistors comprises:

a first transistor of length (L_x) and a width of (W_x); and

a second transistor of length (L_y) and a width of (W_y),

wherein said width-to-length ratio equals $(W_x L_y)/(W_y L_x)$, and

wherein as said input signal decreases, a switching threshold becomes dependent on said width-to-length ratio.

Claim 12 (Canceled).

Claim 13 (Original) The comparator of claim 12, further comprising a plurality of transmission gates in said circuit, wherein said rise in said input signal causes said comparator to appear as a differential pair in an open loop configuration.

Claim 14 (Currently Amended) The comparator of claim 10, wherein in said digital circuit, said input signal is at an input voltage greater than said positive external [reference] voltage

reference.

Claim 15 (Original) The comparator of claim 14, further comprising a plurality of transmission gates in said circuit, wherein said input signal causes said comparator to appear as an asymmetric inverting Schmitt trigger.

Claim 16 (Currently Amended) A comparator for controlling a trip point of a rising and falling edge of an [external] input signal comprising a first portion operatively connected to a second portion, wherein said comparator cycles between an analog circuit and a digital circuit[.], wherein said comparator controls a delay between rising and falling edge transitions at an output signal of said comparator, and wherein said comparator controls a pulse width at said output signal of said comparator.

Claim 17 (Currently Amended) The comparator of claim 16, wherein said analog circuit comprises:

an input signal [source inputting an input signal] terminal;

an output signal [source] terminal;

a positive power supply voltage [source] terminal;

[an] a positive external [input signal source] voltage reference terminal;

a tail current source transistor operatively connected to said positive power supply voltage [source] [source] terminal;

a first pair of transistors operatively connected to said tail current source transistor, said input signal [source] [source] terminal, and said positive external [input signal source] voltage

reference terminal;

a second pair of transistors operatively connected to said first pair of transistors; and

a plurality of invertors operatively connected to said output signal [source] terminal, said first pair of transistors, and said second pair of transistors.

Claim 18 (Currently Amended) The comparator of claim 16, wherein said digital circuit comprises:

an input signal [source inputting an input signal] terminal;

an output signal [source] terminal;

a positive power supply voltage [source] terminal;

a tail current source transistor operatively connected to said positive power supply voltage [source] terminal and said input signal [source] terminal;

a first pair of transistors operatively connected to said tail current source transistor and said input signal [source] terminal;

a current mirror load transistor operatively connected to said input signal source and said first pair of transistors; and

a plurality of invertors operatively connected to said output signal [source] terminal, said first pair of transistors, and said current mirror load transistor.

Claim 19 (Original) The comparator of claim 17, wherein in said analog circuit, said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on.

Claim 20 (Currently Amended) The comparator of claim 18, wherein in said digital circuit, said input signal is at an input voltage greater than said positive external [reference] voltage reference.